ABSTRACT

An output port centric digital data management
architecture for a high speed packet switch employs a dual
key-based content addressable memory (CAM)-based buffer
access control mechanism for efficient storage and read out
of relatively long data packets to one or more output ports
of the switch. The CAM stores respectively different
address pointer words, each containing a respectively
different key field to identify a data packet to be
delivered to a switch output port, and an address field
that identifies the address of one of the storage locations
of the packet buffer in which the data packet is stored.
During a first portion of a dual key CAM search, a packet
request key is coupled to the key fields of all address
pointer words stored in the CAM. The location of the
matching key is used to access the key field's companion
address field in its address pointer word during a second
portion of the dual search of the CAM. During this second
search, the accessed address field is read out so as to
access a data packet stored in the packet buffer, and is
also simultaneously coupled to address fields of all the
address pointer words stored in the CAM. In response to
this second search, the CAM outputs a signal representative
of whether the accessed address field is contained in the
address field of another address pointer word stored in the
CAM, thereby indicating whether or not the buffer address
from which the packet has been accessed is free to store
new data.